REMARKS

102 Rejections

Claims 1-18 are rejected under 35 U.S.C. § 102(b) as being anticipated by Dey et al. (U.S. Patent No. 5,513,123). The Applicants have reviewed the cited reference and respectfully submit that the present invention as is set forth in Claims 1-18 is not anticipated or rendered obvious by Dey et al. (U.S. Patent No. 5,513,123).

The Examiner is respectfully directed to independent Claim 1, which recites that embodiments of the present invention are directed to:

> A method for automatic design of a processor datapath from an input specification including a register file specification, a set of specified processor operations and a desired instruction level parallelism among the specified operations, the method comprising: determining sets of mutually exclusive operations from the specified processor operations based on the desired instruction level parallelism; programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit .....

Independent Claim 10 recites limitations similar to those of independent Claim 1. Claims 2-9 and Claims 11-15 depend from Claims 1 and 10 respectively and recite further limitations of the claimed invention.

Dey et al. does not anticipate or render obvious a method for the automatic design of a processor datapath including "determining mutually exclusive operations from the specified processor operations based on the desired instruction level parallelism" as is recited in Applicants' Claim 1. Dey et al. only shows a non-scan design for testability of RT level data paths. It should be appreciated that the Applicants invention as set forth in Claims 1 and 10 include

limitations that define a relationship between the recited mutually exclusive operations that are determined from specified processor operations, and the recited desired instruction level parallelism. Nowhere in Dey et al. is such a relationship shown or suggested.

Moreover, Dey et al. does not anticipate or render obvious a method for the automatic design of a processor datapath including "programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit." This limitation of Claim 1 and similar limitations of Claim 10 which define a relationship between the recited mutually exclusive operations and the recited corresponding functional unit are nowhere shown or suggested in the Dey et al. reference. Consequently, Dey et al. does not anticipate or render obvious the Applicants' invention as is set forth in Applicants' Claims 1 and 10.

It should be appreciated that not only are the relationships described above not shown or suggested by the Dey et al. reference, but other key related elements of the Applicants' Claims such as the recited "determining mutually exclusive operations" are not taught thereby. Because of such deficiencies Dey et al. does not anticipate or render obvious the Applicants' invention as is set forth in Applicants' Claims 1 and 10.

The Examiner is respectfully directed to independent Claim 16, which recites that embodiments of the present invention are directed to a method for synthesis of a register file including "determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations." Claims 17 and 18 depend from Claims 16 and recite further limitations of the claimed invention.

Dey et al. does not anticipate or render obvious a method for the automatic design of a processor datapath including determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations as is recited in Claim 16. Dey et al. only shows a non-scan design for testability of RT level data paths. Nowhere in the Dey et al. reference is there disclosed a correlation between the sharing of a register port for functional units and the specification of instruction level parallelism. Consequently the Applicants' invention as is set forth in independent Claim 16 is neither shown nor suggested by Dey et al.

The Applicants respectfully submit that the rejection of Claims 1-18 under 35 U.S.C. § 102(b) was in error and respectfully requests the withdrawal of this rejection. The Examiner is reminded that in order to anticipate a Claim, the reference must teach each and every element of the Claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed Cir. 1987). It is clear from the discussion above that "each and every element" is in fact not described by the Dey et al. reference. Dey et al. does not "either expressly or inherently" describe "determining mutually exclusive operations" or "determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations" as was discussed above.

Therefore, Applicants respectfully submit that Dey et al. does not anticipate or render obvious the present claimed invention as recited in claim 1, 10 and 16,

and as such, Claims 1, 10 and 16 are in condition for allowance. Accordingly, Applicants also respectfully submit that Dey et al. does not anticipate or render obvious the present claimed invention as is recited in Claims 2-9 dependent on Claim 1, Claims 11-15 dependent on Claim 10, and Claims 17-18 dependent on Claim 16, and that Claims 2-9, 11-15 and 17-18 traverse the Examiners basis for rejection under 35 U.S.C. 102 as being dependent on an allowable base claim.

Claims 1-5, 7-10, and 12-18 are rejected under 35 U.S.C. § 102(b) as being anticipated by Abbott (U.S. Patent No. 6,351,142). The Applicants have reviewed the cited reference and respectfully submit that the present invention as is set forth in Claims 1-5, 7-10 and 12-18 is not anticipated or rendered obvious by Abbott (U.S. Patent No. 6,351,142).

The Examiner is respectfully directed to independent Claim 1, which recites that embodiments of the present invention are directed to:

> A method for automatic design of a processor datapath from an input specification including a register file specification, a set of specified processor operations and a desired instruction level parallelism among the specified operations, the method comprising: determining sets of mutually exclusive operations from the specified processor operations based on the desired instruction level parallelism; programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit .....

Independent Claim 10 recites limitations similar to those of Claim 1. Claims 2-5 and 7-9, and Claims 12-15 depend from Claims 1 and 10 respectively and recite further limitations of the claimed invention.

Abbott does not anticipate or render obvious a method for the automatic design of a processor datapath including "determining mutually exclusive operations from the specified processor operations based on the desired instruction level parallelism" as is recited in Applicants' Claim 1. Abbott only shows a programmable logic datapath that may be used in a field programmable device. It should be appreciated that the Applicants invention as set forth in Claims 1 and 10 include limitations that define a relationship between the recited mutually exclusive operations that are determined from specified processor operations, and the recited desired instruction level parallelism. Nowhere in Abbott is such a relationship shown or suggested.

Moreover, Abbott does not anticipate or render obvious a method for the automatic design of a processor datapath including "programmatically assigning instances of functional units from a macrocell library to the sets of mutually exclusive operations, such that each specified operation is associated with a corresponding functional unit." This limitation of Claim 1 and similar limitations of Claim 10 which define a relationship between the recited mutually exclusive operations and the recited corresponding functional unit are nowhere shown or suggested in the Abbott reference. Consequently, Abbott does not anticipate or render obvious the Applicants' invention as is set forth in Applicants' Claims 1 and 10.

It should be appreciated that not only are the relationships described above not shown or suggested by the Abbott reference, but other related key elements of the Applicants' Claims such as the recited "determining mutually exclusive operations" are not taught thereby. Because of such deficiencies Abbott does not anticipate or render obvious the Applicants' invention as is set forth in Applicants' Claims 1 and 10.

The Examiner is respectfully directed to independent Claim 16, which recites that embodiments of the present invention are directed to a method for synthesis of a register file comprising "determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations." Claims 17 and 18 depend from Claims 16 and recite further limitations of the claimed invention.

Abbott does not anticipate or render obvious a method for the automatic design of a processor datapath including determining how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations as is recited in Claim 16. Abbott only shows a non-scan design for testability of RT level data paths. Nowhere in the Abbott reference is there disclosed a correlation between the sharing of a register port for functional units and the specification of instruction level parallelism. Consequently the Applicants' invention as is set forth in independent Claim 16 is neither shown nor suggested by Abbott.

The Applicants respectfully submit that the rejection of Claims 1-5, 7-10, and 12-18 under 35 U.S.C. § 102(b) was in error and respectfully requests the withdrawal of this rejection. The Examiner is reminded that in order to anticipate a Claim, the reference must teach each and every element of the Claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed Cir. 1987). It is clear from the discussion above that "each and every element" is in fact not described by the Abbott reference. Abbott does not "either expressly or inherently" describe "determining mutually exclusive operations" or "determining

how to share a register port for two or more functional unit ports based on the specification of instruction level parallelism among the operations" as was discussed above.

Therefore, Applicants respectfully submit that Abbott does not anticipate or render obvious the present claimed invention as recited in claim 1, 10 and 16, and as such, Claims 1, 10 and 16 are in condition for allowance. Accordingly, Applicants also respectfully submit that Abbott does not anticipate or render obvious the present claimed invention as is recited in Claims 2-5, and 7-9 dependent on Claim 1, Claims 12-15 dependent on Claim 10, and Claims 17-18 dependent on Claim 16, and that Claims 2-5, 7-9, 12-15 and 17-18 traverse the Examiners basis for rejection under 35 U.S.C. 102 as being dependent on an allowable base claim.

Conclusion

In light of the above-listed remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Dated: 11/29, 2002

John P. Wagner, Jr.
Registration No. 35,398
Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060